APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

METHOD AND APPARATUS FOR VARYING LENGTHS OF LOW DENSITY PARITY CHECK CODEWORDS

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CROSS-REFERENCE TO RELATED APPLICATIONS.

[0001] This application claims benefit of priority under 35 U.S.C. § 119(e) to U.S. Application 60/536,071, which was filed on January 12, 2004.

BACKGROUND OF THE INVENTION.

[0002] Most communications networks are designed to convey multiple communications simultaneously over each individual communication path, for example, a radio frequency (RF) channel or physical connection, using some type of modulation. In recent years, an increasing demand has arisen for efficient and reliable digital data transfers which assure correct data transmissions at as great a data rate as possible. Forward error correction (FEC) codes have been used in some communications systems for this purpose.

[0003] Codes are essentially digital data sequences derived from message sequences and used to convey message information. In forward error correction (FEC), information may be encoded to provide the abilities of detection and/or correction of errors occurring in a transmission, for example resulting from a noisy channel. The receiver in a communication system can recover all the information in the codewords by itself and thus coding lends advantages to high speed communication systems and/or those requiring synchronous communications.

[0004] Low Density Parity Check (LDPC) codes are a type of FEC block codes which are constructed using a number of simple parity-check relationships shared between the bits in a codeword. An LDPC code (n, k) where n is codeword length and k is the information length, is usually represented by a sparse parity-check matrix H with

dimension n * (n-k). The parity check matrix is used as a basis for encoding and decoding LDPC codewords. LDPC codes are well known for their excellent performance in communications systems but due to their block nature, they have thus far not been flexible enough for systems where either information length or codeword length (or both) is variable. Thus a more flexible LDPC coding scheme is desirable.

BRIEF DESCRIPTION OF THE DRAWING.

[0005] Aspects, features and advantages of the present invention will become apparent from the following description of the invention in reference to the appended drawing in which like numerals denote like elements and in which:

[0006] Fig. 1 is an example matrix showing an example parity check relationship for encoding and decoding information according to various embodiments of the present invention;

[0007] Fig. 2 is a flow diagram illustrating a method for encoding variable length LDPC codewords according to one embodiment of the present invention;

[0008] Fig. 3 is a flow diagram illustrating a method for encoding variable length LDPC codewords according to another embodiment of the present invention;

[0009] Fig. 4 is block diagram of an example communication device according to various aspects of the present invention; and

[0010] Fig. 5 is a block diagram of an example communication network including a communication device similar to that in Fig. 4.

DETAILED DESCRIPTION OF THE INVENTION.

[0011] While the following detailed description may describe example embodiments of the present invention in relation to wireless networks, the embodiments of present

invention are not limited thereto and, for example, can be implemented using wired systems such as Ethernet or Token ring networks and/or optical networks where suitably applicable.

[0012] The following inventive embodiments may be used in a variety of applications including transmitters, receivers and/or transceivers of a radio system, although the present invention is not limited in this respect. Radio systems specifically included within the scope of the present invention include, but are not limited to: wireless local area network (WLAN) systems, wireless metropolitan area network (WMAN) systems and wireless wide area network (WWAN) systems. Related network devices and peripherals such as network interface cards (NICs) and other network adaptors, base stations, access points (APs), gateways, bridges, hubs and cellular radiotelephones are also included. Further, the network systems within the scope of the invention may include cellular radiotelephone systems, satellite systems, personal communication systems (PCS), two-way radio systems, one-way pages, two-way pagers, personal computers (PC), personal digital assistants (PDA), personal computing accessories (PCA) and all future arising systems which may be related in nature and to which the principles of the invention could be suitably applied.

[0013] An LDPC code is a message encoding technique defined by a sparse parity check matrix. The message to be sent is encoded using a generator matrix or the sparse parity check matrix and when it reaches its destination, it is decoded using a related sparse parity check matrix.

[0014] Turning to Fig. 1 a sample parity check matrix 100 H is shown for a (14, 7) code of total codeword length n=14 and information length k=7. The columns of matrix 100

represent code bits and the rows represent parity check equations. As shown, matrix 100 includes a data bit field 105 left of vertical line 112 and a parity bit field 110 right of vertical line 112.

[0015] Conventionally, each LDPC codeword has the same length as others in a block since the block is typically encoded using the same parity check matrix for each codeword. However, according to one embodiment of the present invention, a family of different sized LDPC codes (H matrices) may be used for encoding/decoding different length combinations. For each different size codeword, a corresponding size matrix is used for encoding and decoding. This approach, however, may only be feasible when the number of length combination is relatively small.

[0016] In another approach, turning to Fig. 2, a method 200 for encoding variable length codewords may include determining 205 a length of information to encode in a codeword (and/or determining the size of codeword to be used). If the determined codeword size is less than 210 than a specified size of a default parity check matrix, method 200 may include deleting 215 one or more parity bits of the default matrix or "mother code" to correspond to the size of codeword needed. Method 200 may additionally or alternatively include deleting 220 one or more information bits of the default matrix. A codeword is either encoded 212 based on the default matrix or encoded 225 based on the adjusted matrix.

[0017] Determining the size of the codeword may simply involve identifying a length of information to be sent in each codeword. In one example embodiment, for WLAN, each single medium access control (MAC) service data unit (MSDU) (or MAC protocol data unit (MPDU)) covered by a single CRC checksum is preferably encoded as one

block code. In other words, the data boundary of an MSDU is respected by the encoder. The MSDU length field indicated in a PLCP header, in this embodiment, is all that is needed for identifying the length of the information to be coded.

[0018] The size of the default matrix or "mother code" may be adjusted to accommodate various length combinations by deleting or puncturing code bits. As shown in matrix 100 (Fig. 1), when encoded systematically, the last n-k code bits correspond to parity bits of a codeword and "deleting" or "puncturing" 215 these parity bits is interpreted as erasing these bits in the decoder or setting them as unknown. For a family of low-complexity encodeable parity matrices in the form of $H=[H_1 \mid P]$, where H1 is a low density matrix and P is a lower triangular square matrix, deleting x parity bits may be performed by deleting the last x columns and the last x rows of the H matrix 100 (Fig. 1). As shown by dashed lines 114, 116 in Fig. 1, the original (14, 7) mother code is punctured by 2 parity bits into a (12, 7) code.

[0019] Deleting information bits 220 (in addition to or in lieu of puncturing 215 parity bits) may be performed by deleting columns in data bit field 105 (Fig. 1). Selection of information bit columns for deletion, however, may impact code performance, particularly when accompanied by parity bit puncturing. As shown in the example of Fig. 1, when the two rows under line 116 are deleted, the fourth column in matrix 100 will no longer have any bits remaining (e.g., no "1s" are present in the fourth column of the resized matrix defined by dashed lines 114 and 116). The fourth column is thus no longer represented by any parity check equations in the resized matrix. Accordingly, since the fourth column is the weakest link in resizing matrix 100, it could be beneficial to delete the fourth column first when deleting information bits.

[0020] Generally there are two types of LDPC codes, regular codes and irregular codes. A regular code is represented by a matrix where the column weight for the data bit field is equal for all columns. Conversely, an irregular code is represented by a matrix where column weights may be different from one another. If information bits are to be deleted, method 200 may optionally include identifying or determining 217 one or more of the data bit columns in the mother code having the lowest total bit weight and deleting 220 the one or more columns of the code having the lowest weight. If a regular code is used, the columns may have the same weight unless one or more parity bits are punctured or deleted.

[0021] Referring back to Fig. 1, to derive a (9,4) code from the (12,7) code (e.g., the code after the two parity bits are punctured from the default (14, 7) code), the second, third and fourth columns may be deleted since those columns have the lowest column weight (i.e., number of '1's) after parity bit puncturing. In order to implement this option, however, the column weight distribution may have to be obtained or determined on every instance. This distribution however, may vary with the derived code, i.e., the number of rows deleted. In real-time applications, obtaining this distribution for every case and then selecting columns for deletion on-the-fly may be an inefficient time-consuming procedure.

[0022] Accordingly, in certain embodiments of the present invention, various thresholds may be set to obtain practically achievable results. For example, assume a mother code of (2000, 1600); that is, the H matrix is of size 400 x 2000 for maximum code lengths of 2000 bits of which 1600 may be information bits.

[0023] Turning to Fig. 3, a method 300 for encoding may include using threshold values for handling varying codeword lengths, although the inventive embodiments are not limited to any number of threshold values or code lengths. In one example implementation, two thresholds may be set at 1500 and 1000 although it is entirely discretionary. The length of the code is determined 305 and if the code meets the maximum of the mother code (i.e. 2000) the information is encoded 312 using the full size default parity check matrix as previously discussed.

[0024] When the desired code length is less than 2000 but above 1500 (315), no parity bits are punctured and only information bits are deleted 340 as necessary to accommodate the codeword size. As discussed previously, one or more columns of information bits may be deleted according to a column weight distribution of bits as desired (e.g., if an irregular code is used with no parity bit puncturing).

[0025] In the case of regular codes and no parity bit puncturing, the columns may theoretically have equal weight and thus there may be no need to choose specific information bit columns for deletion since it may not impact code performance. In any event, information for selecting which columns to delete could be previously stored and retrieved 335 such as in a look-up table or other memory.

[0026] For code lengths within the thresholds 1000 and 1500 (320), a number of parity bits may be punctured 325, for example 100 parity bits, and information bits can be deleted according to previously stored column selection information for the case when the last 100 rows are to be deleted due to parity bit puncturing.

[0027] For code lengths less than 1000 a greater number of parity bits such as 150 or 200 could be punctured 330 and previously stored column selection information for

deleting the lowest weighted column(s) of information bits when this many parity bits are punctured can be retrieved 335. The information may then be coded 345 based on the revised parity check matrix. In this manner, only a relatively small amount of information would need to be stored in prior and the complexity of the corresponding encoding system may be reduced while still achieving a reasonable amount of flexibility. Decoding may be performed in a substantially reciprocal manner as that described above using similarly configured algorithms for the decoder.

[0028] Turning to Fig. 4, an example communication device 400 using forward error correction (FEC) with variable length LDPC FEC may generally include a code processing portion 410, and a memory portion 420 accessible by processing portion 410. Device 400 may also optionally include a transceiver/amplifier portion 430 and/or one or more antennas 435. In certain example embodiments, coded information is transmitted/received wirelessly using OFDM modulation and demodulation techniques compatible with one or more Institute for Electrical and Electronic Engineers (IEEE) 802.11 standards for wireless local area networks (WLANs), although the inventive embodiments are not limited in this respect. (Note: two antennas are shown in Fig. 4 for optional Multiple Input Multiple Output (MIMO) implementations).

[0029] Memory portion 420 may include one or more fixed, removable, internal or external memories and capable of storing machine readable code and/or other data which may be used by processing portion 410, for example to perform one or more of the variable length LDPC encoding/decoding processes described herein. Processing portion 410 and/or memory portion 420 may be any single component or combination of components for performing these functions.

[0030] Processing portion 410 may be configured to perform digital communication functions such as a medium access control 412 and/or baseband processing 414. In one example implementation, an LDPC encoder/decoder 415 configured to perform one of the previously described variable length encoding methods is integrated, along with an optional digital demodulator (not separately shown), as part of a digital baseband processor 414. The inventive embodiments are however not limited in this respect. Additional elements, such as one or more analog to digital converters (ADC), digital to analog converters (DAC), a memory controller, a digital modulator and/or other associated elements, may also be included as part of device 400.

[0031] In certain embodiments, processing portion 410 and/or memory portion 420 may be implemented using one or more programmable devices such as a microprocessor, Digital Signal Processor (DSP), microcontroller or field programmable gate array. Additionally and/or alternatively, various elements of processing portion 410 may be implemented using discrete circuit components or as one or more application specific integrated circuits (ASICs). Other implementations may also be possible and the principles of the inventive embodiments are not limited to any specific hardware, software or firmware implementation.

[0032] Referring to Fig. 5, an example communication network 500 using variable length LDPC codes for forward error correction (FEC), and for which the inventive embodiments may be adapted, may include one or more wireless network access stations 505 and one or more wireless user stations 507-509. Wireless network access station 505 may be any device or combination of devices which facilitate network access to wireless user stations 507-509 via electromagnetic waves including for

example, a wireless local area network (WLAN) access point (AP), a wireless wide area network (WWAN) AP, a cellular telephone base station and the like. User stations 507-509 may be any device or component of such device configured to communicate with access station 505, including for example, a cellular telephone 507, a laptop computer 508, a personal digital assistant 509 or other communication or computing devices and/or their RF interfaces.

[0033] Network access station 505 may include and/or be communicatively coupled to a network processor 520 such as a network server, telephone circuit switch, or any other packet or frame-based network switch and/or information control device. Network 500 may additionally or alternatively include physically connected components such as those used in a wired network (e.g., Ethernet 525 and related user stations 528, 529) or a fiber optic network (e.g., fiber optic transceiver 530). Accordingly, any device in network 500 using FEC may suitably include encoding/decoding components arranged to perform the variable length LDPC coding methods described herein.

[0034] Unless contrary to physical possibility, the inventor envision the methods described herein: (i) may be performed in any sequence and/or in any combination; and (ii) the components of respective embodiments combined in any manner.

[0035] Although there have been described preferred embodiments of this novel invention, many variations and modifications are possible without departing from the scope of the invention and the embodiments described herein are not limited by the specific disclosure above, but rather should be limited only by the scope of the appended claims and their legal equivalents.